

The diagram shows a cross-section of a semiconductor processing chamber. At the top, a wafer W is held between two parallel plates or electrodes, labeled 41 and 42. Gas flows from left to right, as indicated by arrows, entering through a port 32 and exiting through a vent 31. Various electrical connections are shown, including a switch SW1, coils L1, capacitors C1, and a controller 8. Other labels include 2, 3, 4, 21, 22, 23, 24, 25, 30, 31, 32, 40, 41a, 42, 43, 43a, 44, 45, 46, 47, 51, 52, 53, 54, 55a, 56, and 57.

FIG. 2

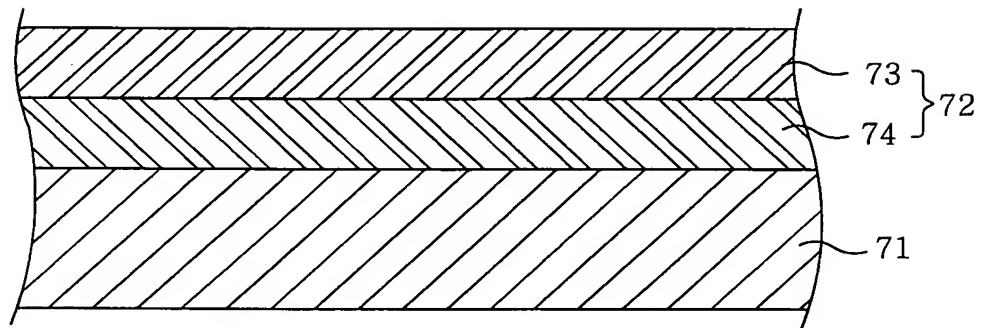


FIG. 3

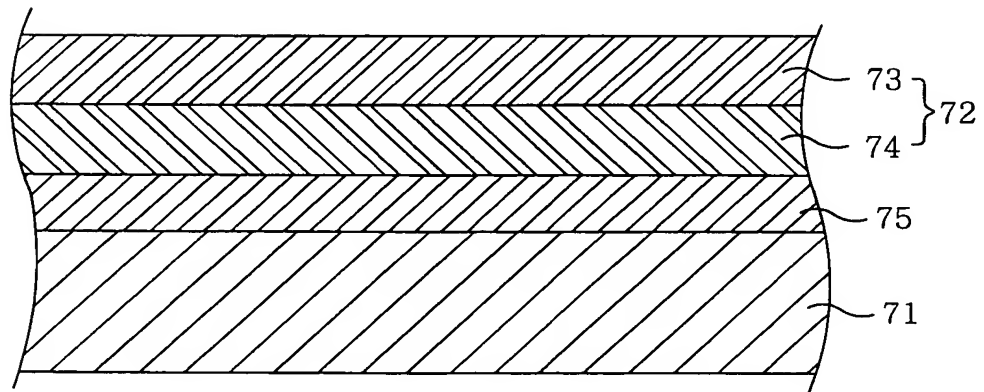


FIG. 4A

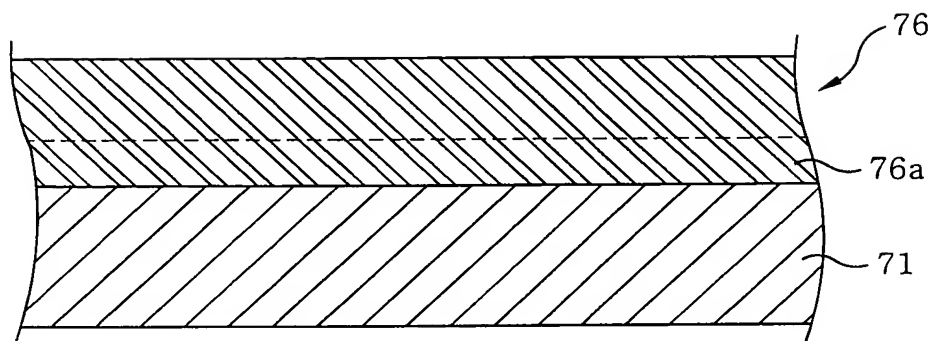


FIG. 4B

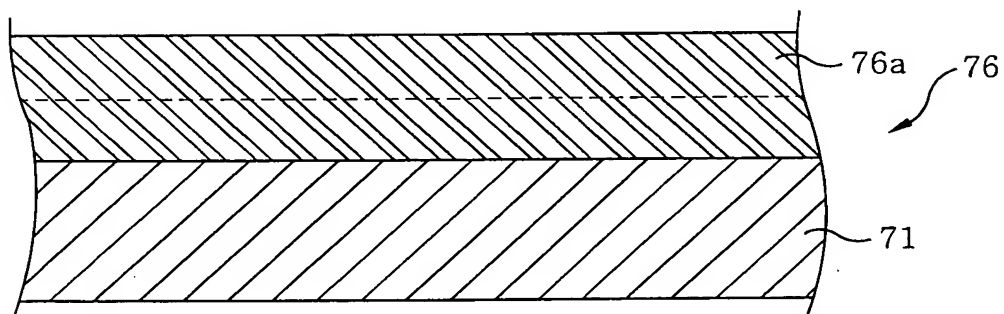


FIG. 4C

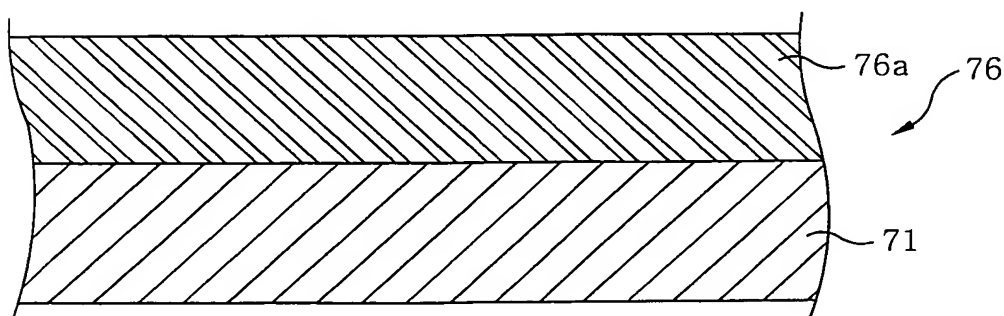


FIG. 5

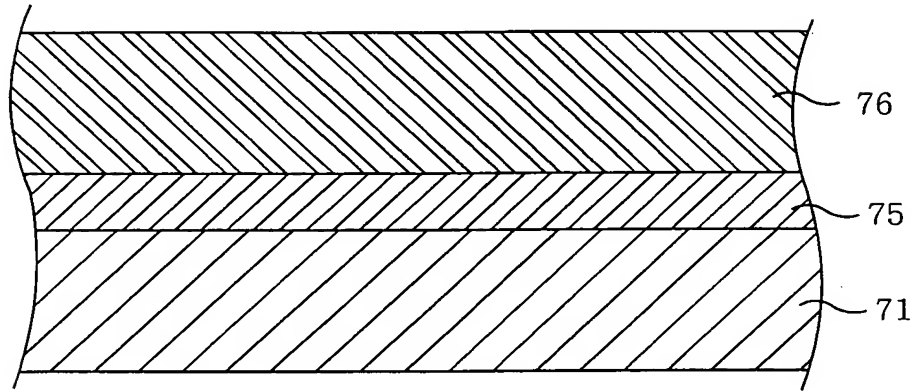


FIG. 6A

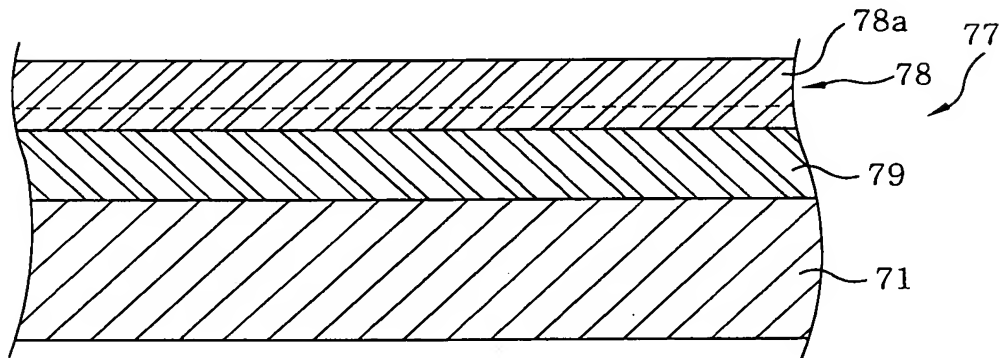


FIG. 6B

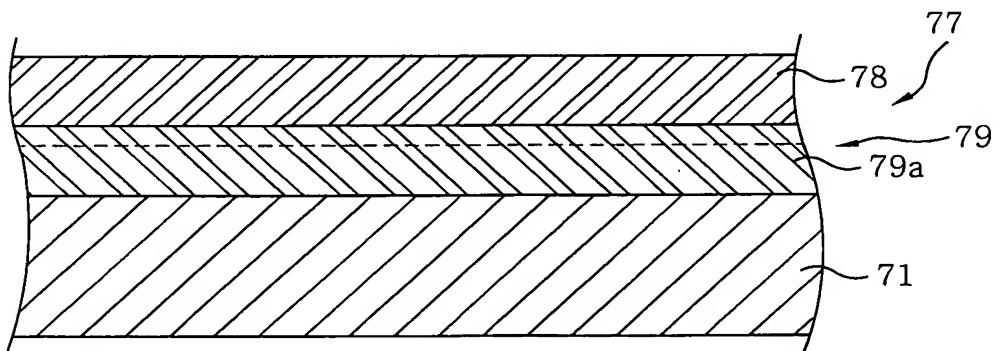


FIG. 7

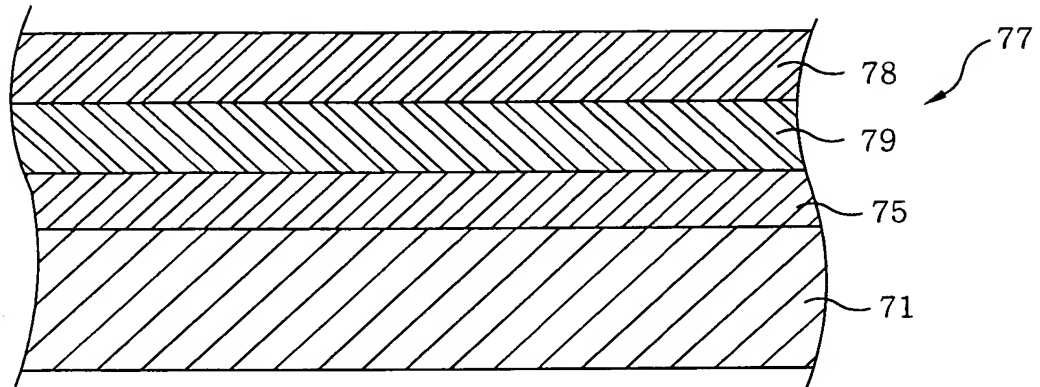


FIG. 8

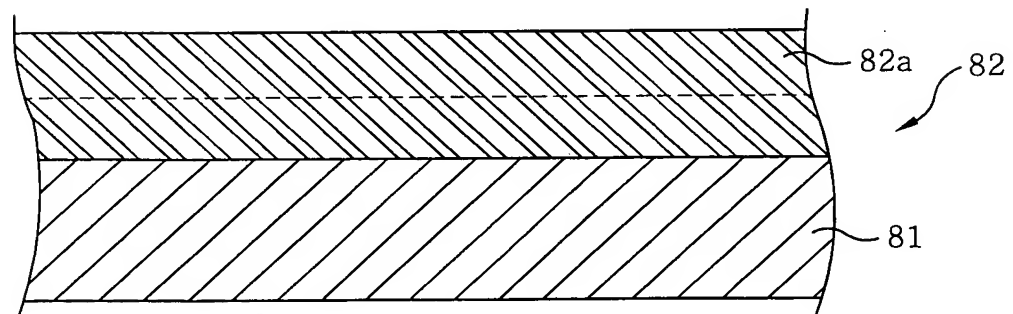


FIG. 9A

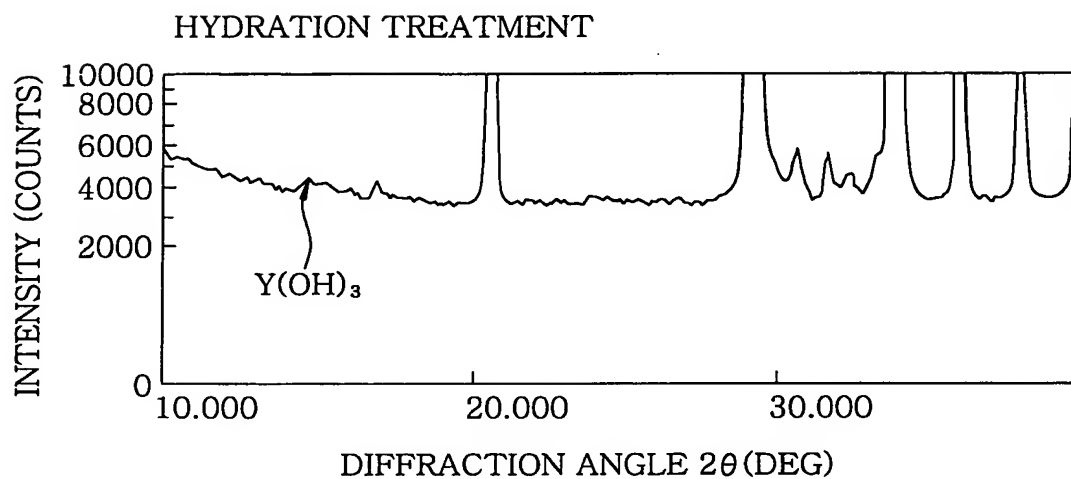


FIG. 9B

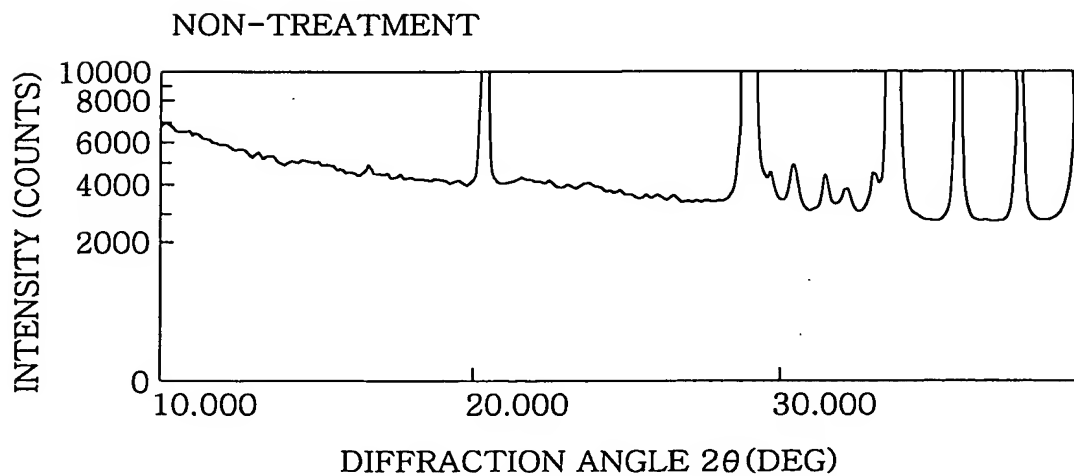


FIG. 10

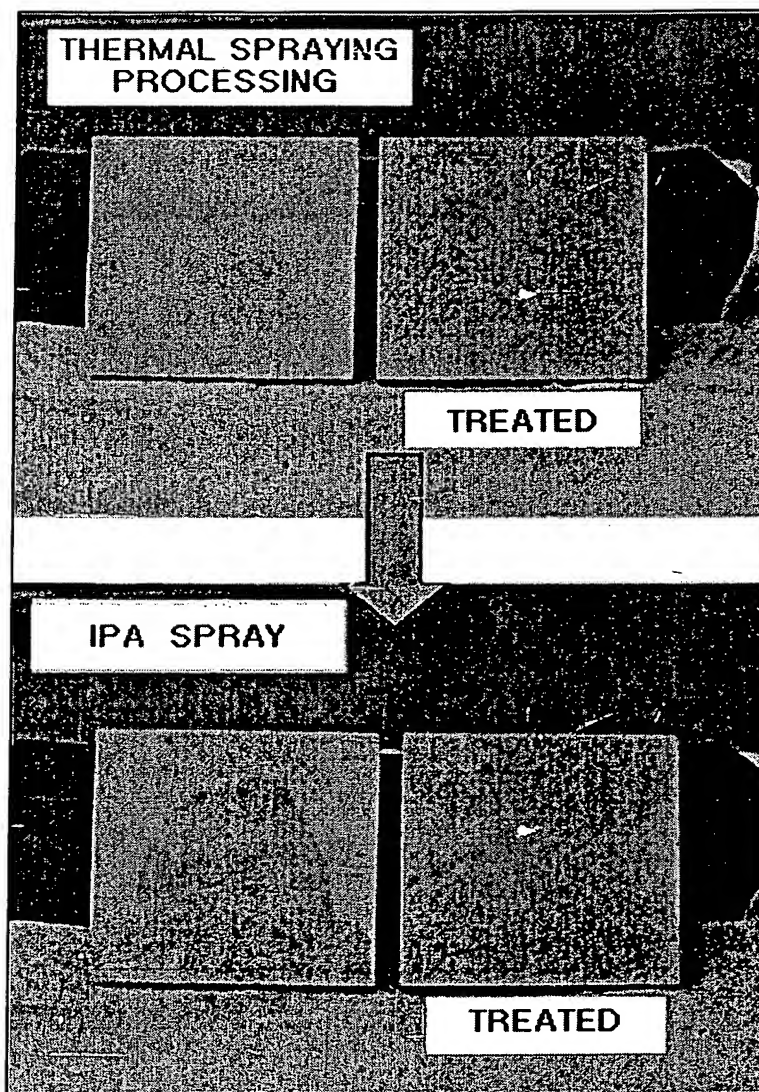


FIG. 11A

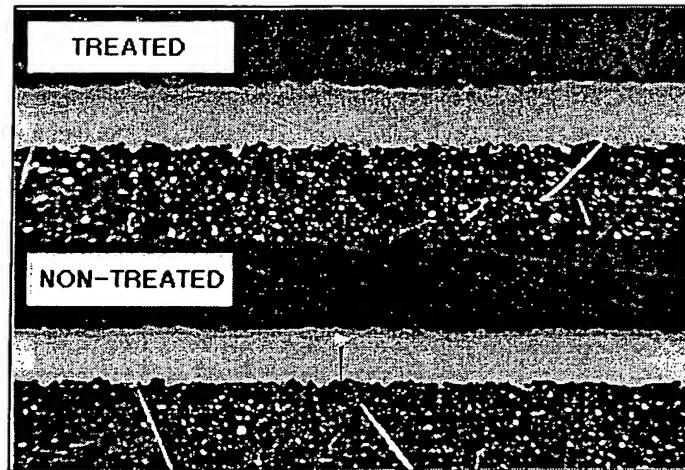


FIG. 11B

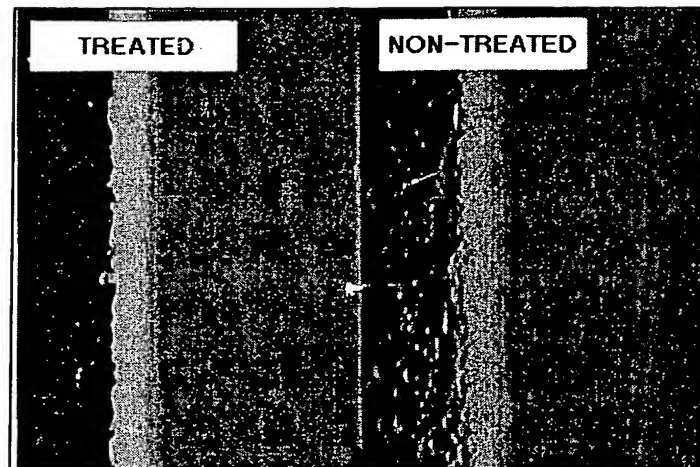


FIG. 11C

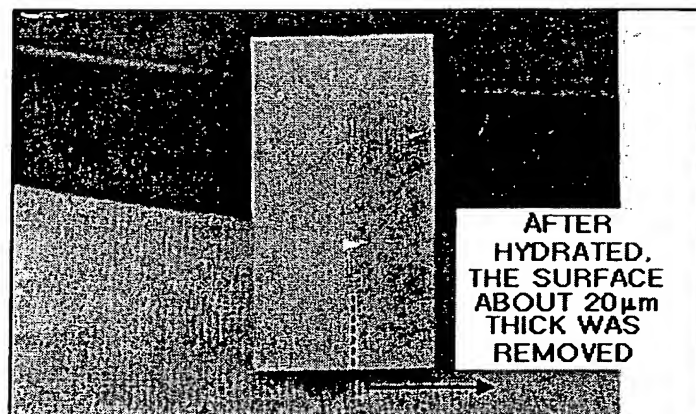


FIG. 12A

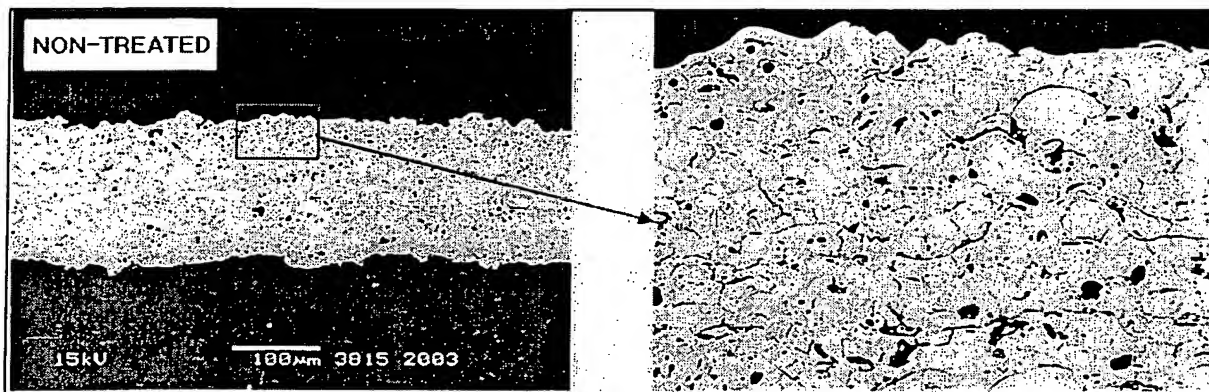


FIG. 12B

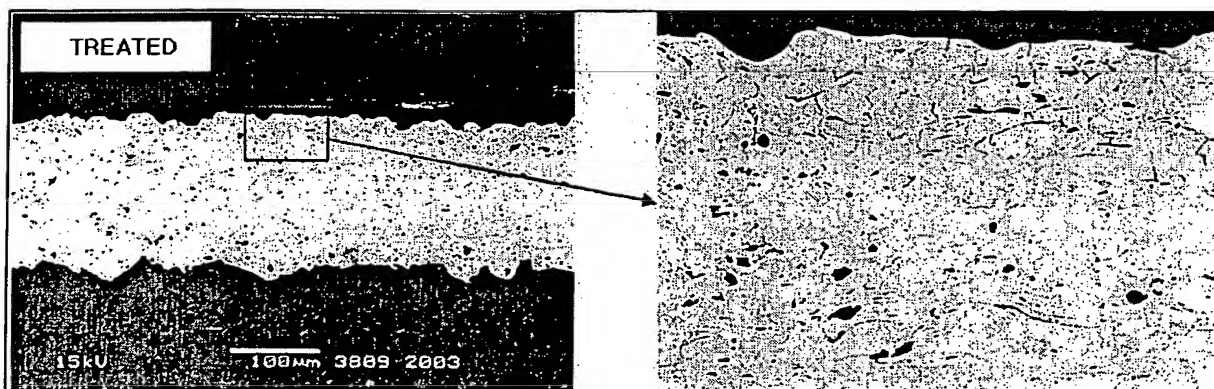


FIG. 13

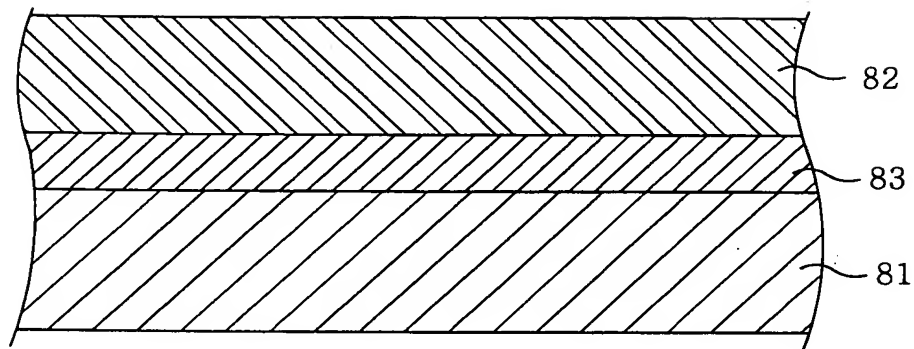


FIG. 14A

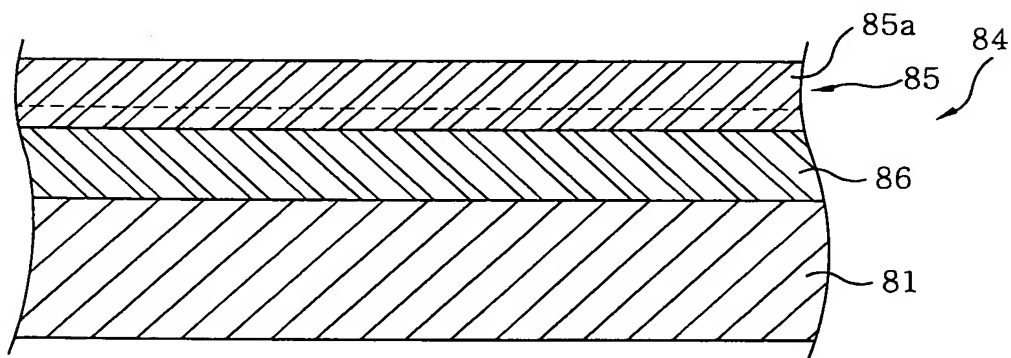


FIG. 14B

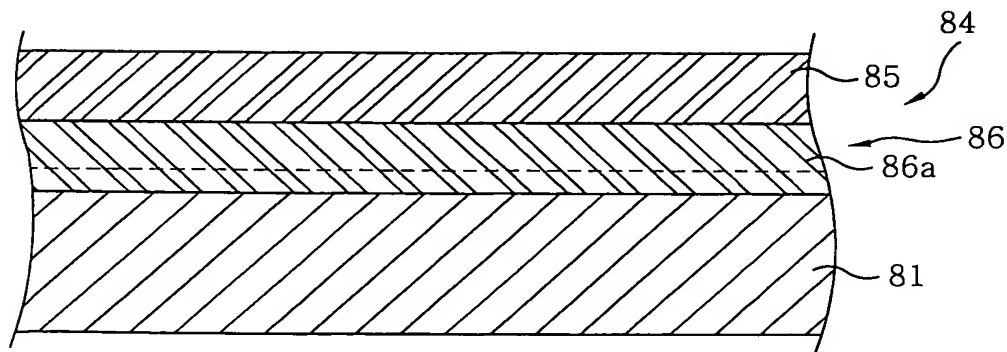


FIG. 15

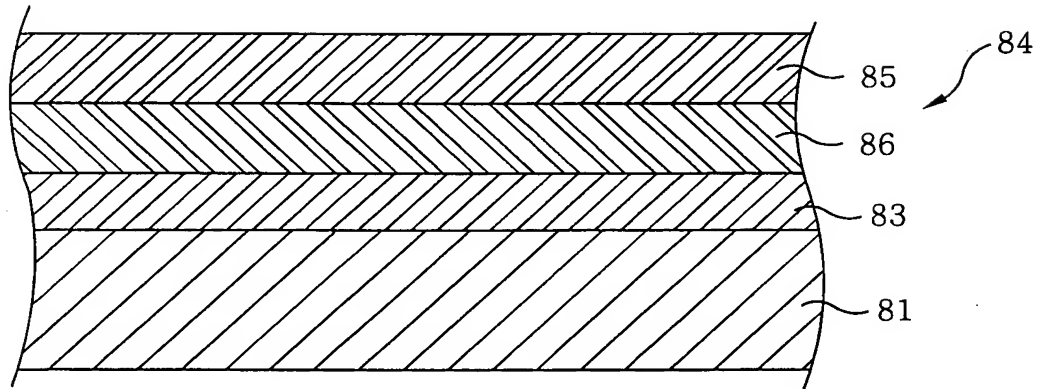


FIG. 16

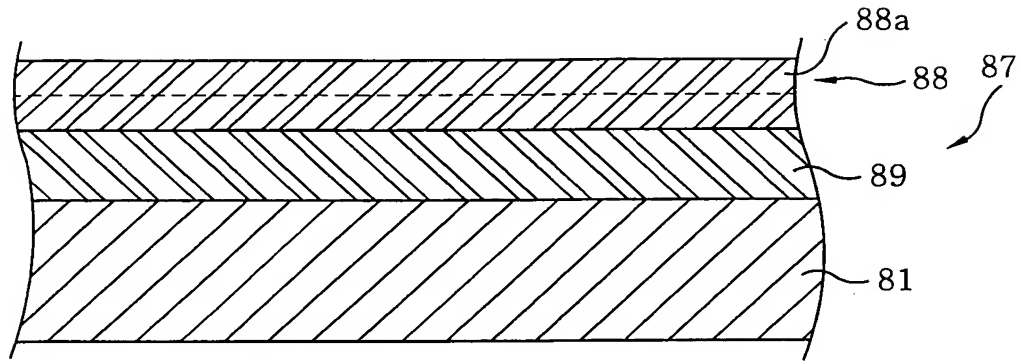


FIG. 17

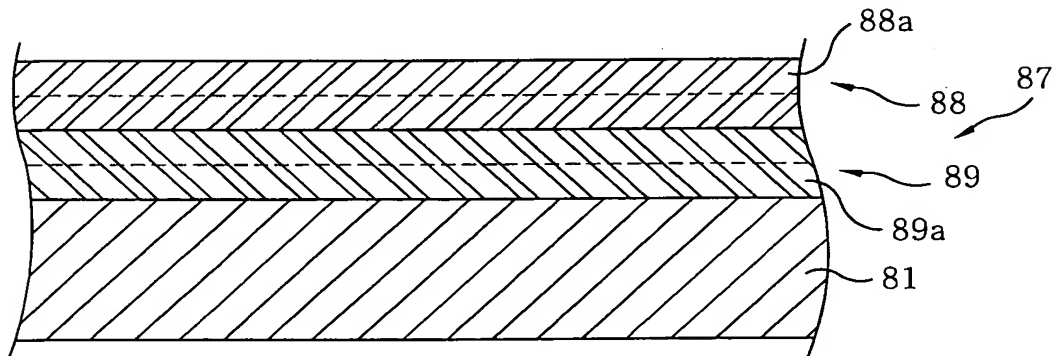


FIG. 18

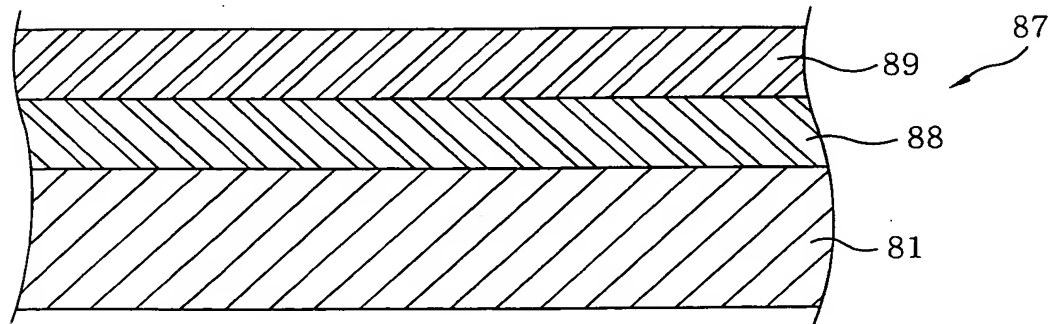


FIG. 19

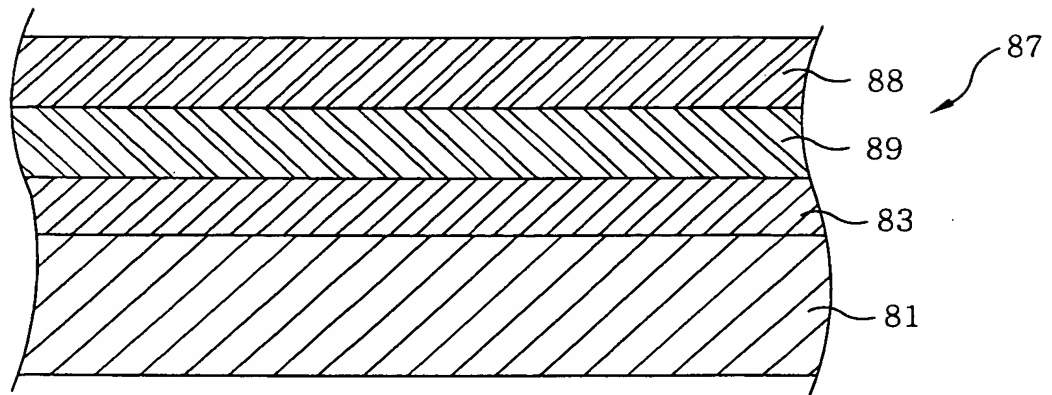


FIG. 20

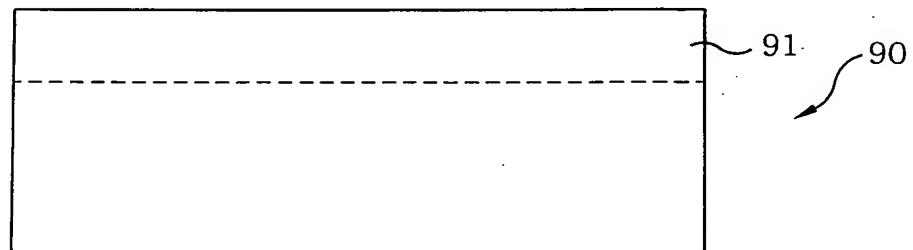


FIG. 21A
(PRIOR ART)

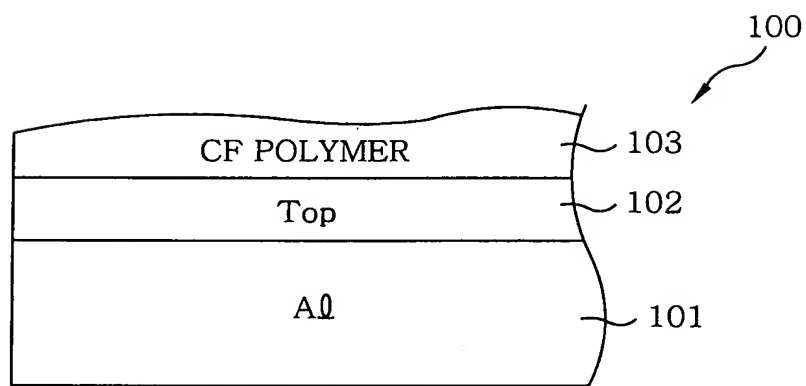


FIG. 21B
(PRIOR ART)

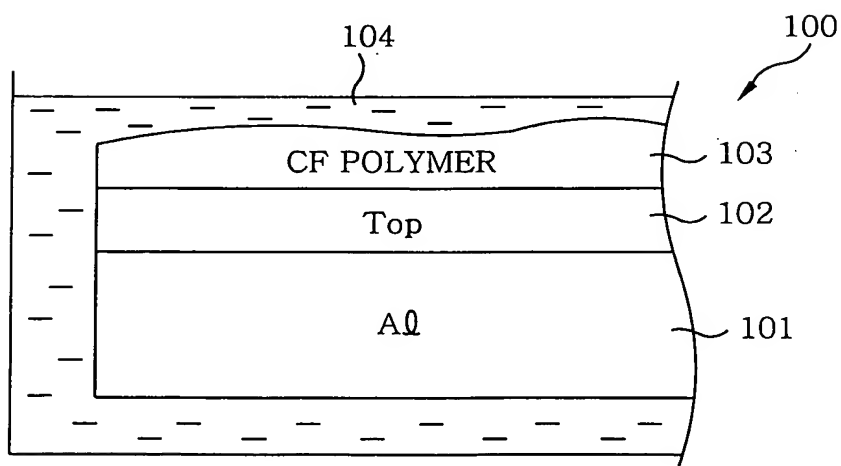


FIG. 21C
(PRIOR ART)

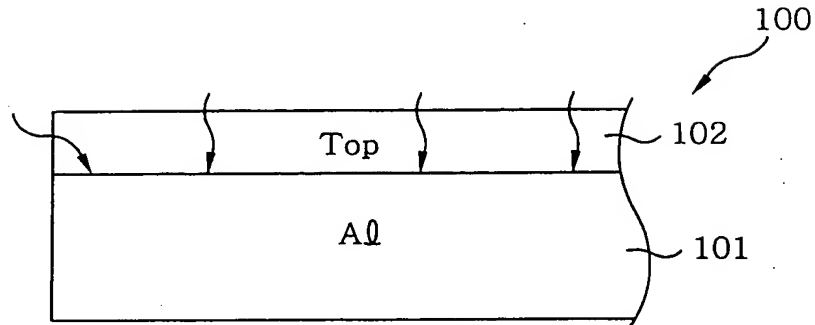


FIG. 21D
(PRIOR ART)

